Patent claims

1. A rewiring substrate strip with several semiconductor component positions (2) for semiconductor components (3) which are arranged in semiconductor chips (4) arranged in several component rows (29) and component columns (30) subdivided by cutting lines (12), wherein several semiconductor components positions (2) are combined to form one component group (5), the component group (5) comprising several semiconductor chips (4) of the semiconductor components (3) on a top side (31) of the rewiring substrate strip (100), and wherein cutting strips (18) which have test contact surfaces (13) are provided between the component rows (29) and component columns (30) within a component group (5), the semiconductor component positions (2) and the test contact surfaces (13) being aligned with respect to one another in such a manner that a parketting pattern according to a parallel-rod Parquet pattern is produced and the arrangements of external contacts (9) and test contact surfaces (13) on the rear side (6) of the rewiring substrate strip (100) are correspondingly aligned with respect to one another in such a manner that the arrangements of four next neighbors of a semiconductor component (3) are rotated by uniformly 90° or by uniformly 270° with respect to the one arrangement in accordance with a predetermined plan.

2. The rewiring substrate strip according to claim 1, characterized in that the component rows (29) and component columns (30) comprise first and second semiconductor chips (41, 42), the first and second semiconductor chips (41, 42) differing in their alignments (A, B) and the first semiconductor chips (41) having a first alignment (A) and the second semiconductor chips (42) having a second alignment (B) rotated uniformly by 90° or uniformly by 270° with

respect to the first alignment A, and the first and second semiconductor chips (41, 42) being arranged alternately in the component rows (29) and component columns (30).

3. The rewiring substrate strip according to claim 1 or claim 2, characterized in that on a rear side (6), opposite to the top side (31), of the rewiring substrate strip (100) external contact patches (10) having external contacts (9) are arranged in the semiconductor component positions (2) and wherein the external contact patches (10) are electrically connected to the test contact surfaces (13) on the cutting strips (18) via rewiring lines.

4. The rewiring substrate strip according to one of the preceding claims, characterized in that in the semiconductor component positions (2), the test contact surfaces (13) on cutting strip sections which are arranged at two opposite edges (22) of the semiconductor components (3) are allocated to the respective semiconductor component position (2).

5. The rewiring substrate strip according to one of the preceding claims, characterized in that the cutting strips (18) are arranged horizontally along the component rows (29) and vertically along the component columns (30), and in each case form an intersection area (32) which comprises a number of test contact surfaces (13), a quarter of these test contact surfaces (13) on an intersection area (32) in each case being allocated to one of the four adjoining semiconductor component positions (2).

6. The rewiring substrate strip according to one of the preceding claims, characterized in that one or more component groups (5) are arranged in a row behind one another and/or next to one another on the rewiring

substrate strip (100) and preferably have one or more plastic covers (17).

7. The rewiring substrate strip according to one of the preceding claims, characterized in that in the semiconductor component positions (2), external contact patches (10) having external contacts (9) are arranged in an external contact patch matrix with external contact rows (11) and external contact columns (14).

8. The rewiring substrate strip according to one of the preceding claims, characterized in that the semiconductor chips (4) are electrically connected to the rewiring substrate strip (100) via flip chip contacts or via bonding wire connections.

9. The rewiring substrate strip according to one of the preceding claims, characterized in that the rewiring substrate strip (100) has on its rear side (6), outside the area (26) of a component group (5), areas with exposed test contact surfaces, the test contact surfaces being electrically connected to the test contact surfaces (13) in the cutting strips (18) and/or the external contact patches (10) of the semiconductor components (3) via rewiring lines.

10. The rewiring substrate strip according to one of the preceding claims, characterized in that the rewiring substrate strip (100) has in an edge area (15) a plug-in contact strip (16) with plug-in contact surfaces, the plug-in contact surfaces being electrically connected to the test contact surfaces (13) and/or to test contact surfaces and/or the external contact patches (10).

11. The rewiring substrate strip according to claim 10, characterized in that the plug-in contact strip (16) of the rewiring substrate strip (100) is provided

for a temperature cycle test or, respectively, "burn-in" test.

12. The rewiring substrate strip according to one of the preceding claims, characterized in that the test contact surfaces (13) carry test contacts (19).

13. The rewiring substrate strip according to one of the preceding claims, characterized in that the test contact surfaces (13) comprise gold plating.

14. The rewiring substrate strip according to one of the preceding claims, characterized in that the rewiring substrate strip (100) has in the semiconductor component positions (2) stacks of a logic chip and a memory chip, wherein both the memory functions of the memory chip and the logic functions of the logic chip can be tested via test contact surfaces (13) and/or via exposed test contact surfaces and/or via test contacts (19) and/or via plug-in contact strips (16).

15. A semiconductor component which is formed by separating the rewiring substrate strip (100) according to one of claims 1 to 14 and thus comprises on opposite edges (22) cut rewiring lines which led to test contact surfaces (13) on cutting strips (18) of the rewiring substrate strip (100).

16. A method for producing a rewiring substrate strip (100) with several component groups (5), wherein the component groups (5) comprise semiconductor component positions (2) with semiconductor chips (4), the semiconductor component positions (2) being arranged in component rows (29) in the x-direction and in component columns (30) in the y-direction, and wherein the method comprises the following method steps;

- providing a substrate strip (23) which is metal-plated on its rear side (6),

- applying a rewiring structure on the metal-plated substrate strip (23), the rewiring structure comprising external contact patches (10) in the semiconductor component positions (2) and test contact surfaces (13) in the area (8) of cutting strips (18) between the semiconductor component positions (2),
- mounting semiconductor chips (4) on the top side (31) of the rewiring substrate strip (100) in the semiconductor component positions (2), in such a manner that first each odd-numbered semiconductor component position (2) in the component rows (29) and component columns (30) is equipped with a first semiconductor chip (41) in a first alignment (A) and then the remaining even-numbered semiconductor component positions (2) are equipped with a second semiconductor chip (42) in a second alignment (B) which is rotated uniformly by 90° or uniformly by 270° with respect to the first alignment (A), so that a rod-Parquet pattern is formed in accordance with a predetermined plan in the x- and y-direction,
- producing connections between the semiconductor chips (4) and the rewiring structure,
- applying external contacts (9) in the semiconductor component positions (2) to the external contact patches (10) of the rewiring structure on the rear side (6) of the rewiring substrate strip (100),
- performing functional tests of the semiconductor chips (4), combined into component groups (5), by contacting the test contact surfaces (13),
- marking defective semiconductor components (3) on the rewiring substrate strip (100).

17. The method according to claim 16, characterized in that the semiconductor chips (4) are mounted uniformly and with standard alignment on the top side (31) of the

rewiring substrate strip (100) and a rewiring structure is provided on the rewiring lines which provides in the semiconductor component positions (2) of the rewiring substrate strip (100) an alignment of the arrangement of external contacts (9) which is rotated uniformly by 0° and/or 180° for odd-numbered semiconductor component positions (2) with respect to the alignment of the semiconductor chips in the component rows (29) and the component columns (30) and rotated uniformly by 90° and/or uniformly by 270° with respect to the alignment of the semiconductor chips for even-numbered semiconductor component positions (2), so that the predetermined rotation in the semiconductor component positions (2) is carried out by means of a predetermined redistribution plan for a multi-layered rewiring substrate strip (100).

18. The method according to claim 16, characterized in that, for mounting differently aligned and arranged semiconductor chips (4) on the rewiring substrate strip (100), a wafer separated into semiconductor chips (4) is available which comprises semiconductor chips (4) aligned and arranged in a preparatory manner in an x- and y-arrangement and in rotational alignment, which are mounted on the top side (31) of the rewiring substrate strip (100) in this predetermined arrangement and alignment of the wafer by an automatic insertion machine.

19. The method according to claim 16, characterized in that, for mounting differently aligned and arranged semiconductor chips (4) on the rewiring substrate strip (100), a foil with semiconductor chips (4) is available which comprises semiconductor chips (4) aligned and arranged in a preparatory manner in the x- and y-arrangement and in rotational alignment, which are mounted on the top side (31) of the rewiring substrate

strip (100) in this predetermined arrangement and alignment by an automatic insertion machine.

20. The method according to claim 16, characterized in that, for mounting differently aligned and arranged semiconductor chips (4) on the rewiring substrate strip (100), an automatic insertion machine which is programmable in x-, y-arrangement and rotational alignment, is used which picks up semiconductor chips (4) arranged in standard manner and uniformly aligned from a wafer separated into semiconductor chips (4) or from a foil uniformly equipped with semiconductor chips (4) and which carries out the provided arrangement and alignment plan according to program during the equipping of the rewiring substrate strip (100).

21. The method according to one of claims 16 to 20, characterized in that the semiconductor chips (4) in the component groups (5) are semiconductor chips (4) with flip chip contacts and connections between semiconductor chips (4) and a rewiring structure are established on the top side (31) of the rewiring substrate strip (100) by means of a soldering process.

22. The method according to one of claims 16 to 20, characterized in that the semiconductor chips (4) are mounted with their rear sides on the semiconductor component positions (2) and connections between semiconductor chips (4) and a rewiring structure on the top side (31) of the rewiring substrate strip (100) are established by means of bonding technology.

23. The method according to one of claims 16 to 22, characterized in that, after the connections are established between semiconductor chips (4) and rewiring substrate strip (100), plastic covers (17) are applied to the component groups (5) which embed the semiconductor chips (4) in a plastic compound.

24. The method according to one of claims 16 to 23, characterized in that the test contact surfaces (13) and/or the external contact patches (10) of the rewiring structure are selectively plated with a gold alloy.

25. The method according to one of claims 16 to 24, characterized in that solder balls (28) are soldered to the test contact surfaces (13) as test contacts (19).

26. A method for producing semiconductor components (3) which comprises the following method steps:

- producing a rewiring substrate strip (100) according to one of claims 16 to 25,
- separating the rewiring substrate strip (100) into individual components and,
- sorting out the semiconductor components (3) marked as defective.